REMARKS

Status of the Claims

- Claims 1, 4, 6, 9, and 11-13 are pending in the Application.
- Claims 1, 4, 6, 9, and 11-13 are rejected by Examiner.

Claim Rejections Pursuant to 35 U.S.C. §103

Claims 1, 4, 6, and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Profibus Technical Description Order No. 4.002, September 1999, (Profibus) in view of U.S. Patent No. 6,073,244 to Iwazaki. Applicant respectfully traverses the rejection.

Profibus describes a process field bus having freeze and sync modes. These modes are used in for event-controlled synchronization of slaves operating in a Profibus architecture. Profibus at page 15, col. 2 second paragraph states:

"The slaves begin sync mode when they receive a sync command from their assigned master. The outputs of all addressed slaves are then frozen in their current state. During subsequent user data transmissions, the output data are then stored at the slaves, but the output states remain unchanged. The stored output data are not sent to the outputs until the next sync command is received. Sync mode is concluded with the unsync command." (Profibus, p. 15, col 2).

Thus, in Profibus, the masters send a sync command to the slaves in order to freeze the output states. User data is then sent to the slaves to be stored, and a second sync command is used to transfer the stored data to the slave outputs.

Applicant notes that that Profibus requires a reasonably stable and continuous clock. In synchronizing applications between Masters and Slaves on Profibus, typical clock jitter must be less than 1 microsecond. As stated in Profibus at page 31, col. 2, last paragraph:

" For typical applications, the jitter of the clock signal from cycle to cycle *must* be less than 1 us. Larger deviations are regarded as cycle failures and are not processed. If one cycle is omitted, the following cycle *must* be within the time frame again. The system clock is set by the user in the course of bus configuration." (See Profibus, page 31).

Applicant respectfully submits that one of skill in the art would interpret the above paragraph in the Profibus technical description as requiring a stable and continuous clock for proper operation. If clock cycles are missing or stopped, (i.e. detected as a large deviation of the jitter specification), then the jitter specification is exceeded and it is regarded as a cycle failure resulting in a halt in processing according to the Profibus technical description on page 31.

Thus, Applicant concludes that Profibus, by itself, teaches away from the present claims because Profibus requires a continuous clock whereas pending independent Claims 1 and 6 recite a transfer pulse that occurs when transitions of the clock signal are not present on the clock line (i.e. when the clock is absent or has stopped).

The present Office Action dated 12/01/2008 indicates on page 4 that "...Profibus does not explicitly disclose that it is via the bus connection...having a data line, a control line, and a clock line," "sending a start pulse signaling a start of a data transmission from the central IC to the peripheral IC via the control line", or "wherein the start pulse is transmitted on the control line during a first phase where transitions of the clock signal are present on the clock line and wherein the transfer pulse is transmitted on the control line in a second phase where transitions of the clock signal are not present on the clock line." Applicant agrees. However, Applicant respectfully disagrees that the combination of Profibus and Iwazaki discloses all of these claimed elements.

Iwazaki discusses a power saving clock control apparatus and method. Iwazaki at Figure 2 illustrates a unit protocol. Figure 2A is the clock input to the central processing unit (CPU). Figure 2B is a start signal output from the CPU. Figure 2C is an address signal output from the CPU. Figure 2D is a control

signal output from the CPU. Figure 2E is a data output from the CPU. Figure 2F is a separate bus end signal output of the CPU. (See Iwazaki, Figure 2, col. 6, lines 16-26).

Applicant notes that the clock signal of Iwazaki Figure 2A is shown to have continuous transitions throughout the entire illustrated protocol. In order for the configuration of Iwazaki to operate to change a clock selection unit (41) frequency setting, a continuous clock is needed to complete the protocol transfer mechanism of Figures 2A-2F. Without a completion of the protocol of Figures 2A-2F (including the continuous clock), there would be no change in the clock frequency unit in Iwazaki. Applicant respectfully submits that one of skill in the art would recognize that a continuous clock is required in Iwazaki to complete a transfer of data into a clock selection control unit. Thus, any frequency change in Iwazaki can only result after the continuous clock protocol of Iwazaki shown in Figures 2A-2F.

In addition, Applicant notes that each of the Iwazaki pulses of Figures 2B, 2C, and 2F have a period that is visibly longer than the clock period of Figure 2A. Therefore, one of skill in the art would recognize that pulses of Figures 2B, 2D, and 2F occur, in full duration, when transitions of the clock of Figure 2A are occurring. That is, the clock signal of Figure 2A transitions during the occurrence of any of the pulses. Thus, Iwazaki Figures 2A-2F teach against the pending claims which recite that a transfer of data occurs during a second phase where there are no transitions on the clock line.

Since Figures 2A-2F show a continuous clock throughout the entire protocol duration, then Applicant respectfully submits that Iwazaki Figures 2A-2F fail to disclose the aspect that "wherein the transfer pulse is transmitted on the control line in a second phase where transitions of the clock signal are not present on the clock line" as recited in pending independent Claims 1 and 6.

Also, since Iwazaki teaches that a continuous clock is needed to complete a transfer of information to a clock selection control unit, then Iwazaki

also teaches away from the currently claimed invention which recites that "the transfer pulse is transmitted on the control line in a second phase where transitions of the clock signal are not present on the clock line".

Applicant respectfully submits that both Profibus and Iwazaki teach that a continuous clock is required for proper operation of the Profibus and Iwazaki configurations. This teaches away from the pending independent Claims 1 and 6 as described above. Thus, the combination of Profibus and Iwazaki teaches away from the pending claims as well as fails to teach or suggest at least the claimed aspect that "the transfer pulse is transmitted on the control line in a second phase where transitions of the clock signal are not present on the clock line". Thus, the combination of Profibus and Iwazaki cannot form a prima facie case of obviousness under 35 USC §103(a) because the references teach away from the claimed invention and because the combination fails to teach or suggest all of the elements of independent Claims 1 and 6. Claims 4 and 9 are dependent on patentably distinct Claims 1 and 6 respectively and thus are also rendered non-obvious under 35 USC §103(a) per MPEP §2143.03.

Applicant respectfully requests reconsideration and withdrawal of the 35 USC §103(a) rejections on Claims 1, 4, 6, and 9 in light of the arguments presented above.

Claims 11-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Profibus Technical Description Order No. 4.002, September 1999, (Profibus) in view of U.S. Patent No. 6,073,244 to Iwazaki and in further view of U.S. Patent No. 7,120,427 to Adams et al. (Adams). Applicant respectfully traverses the rejection via amendment of independent Claim 6.

The teachings of Profibus and Iwazaki are presented above. Applicant notes that the combination of Profibus and Iwazaki fails to establish a prima facie case of obviousness against pending amended independent Claim 6, upon which Claims 11-13 depend, because the combination of Profibus and Iwazaki fails to teach or suggest all of the elements of independent Claim 6 and

the combination actually teaches away from the claimed invention. The addition of Adams to the combination of Profibus and Iwazaki does not change that result. Adams fails to teach the elements missing from the combination of Profibus and Iwazaki. Adams also cannot cure the aspect that the combination of Profibus and Iwazaki teaches away from the pending claims. Accordingly, Claims 11-13 are not rendered obvious by the combination of Profibus, Iwazaki, and Adams per MPEP §2143.03.

Applicant respectfully requests reconsideration and withdrawal of the 35 USC §103(a) rejections on Claims 11-13 in light of the amendment to independent Claim 6 and the arguments presented above.

Conclusion

Applicant respectfully submits that the pending claims patentably define over the cited art and respectfully requests reconsideration and withdrawal of all rejections of the pending claims.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 07-0832 therefore.

Respectfully submitted,
Friedrich Heizmann et al.

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/Jerome G. Schaefer/
Jerome G. Schaefer
Attorney for Applicants
Reg. No. 50,800
(609) 734-6451

Thomson Licensing, LLC
Patent Operation
PO Box 5312
Princeton, NJ 08543-5312